JC07 Rec'd PCT/PTO 15 NOV 2001

FORM PTO-1390
REV. 5-93

US DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEYS DOCKET NUMBER: P01,0345

U.S.APPLICATION NO. (if known, see 37 CFR 1.5): 09/980317

NTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/DE00/01497	11 May 2000	20 May 1999

TITLE OF INVENTION: "SUBSTRATE WITH AT LEAST TWO METALLIZED POLYMER BUMPS FOR SOLDERED CONNECTION TO WIRING"

APPLICANT(S) FOR DO/EO/US: Jozef van Puymbroeck

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay.
4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.

5. ☒ A copy of International Application as filed (35 U.S.C. 371(c)(2))
   a. ☒ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US)
6. ☒ A translation of the International Application into English (35 U.S.C. 371(c)(2).

7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. §371(c)(3))
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.

8. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).

9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).

10. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11. to 16. below concern other document(s) or information included:

11. ☒ An Information Disclosure Statement under 37 C.F.R. 1.97 and 1.98; **(PTO 1449, Prior Art, Search Report)**.

12. ☒ An assignment document for recording. A separate cover sheet in compliance with 37 C.F.R. 3.28 and 3.31 is included.
    (SEE ATTACHED ENVELOPE)

13. ☒ A FIRST preliminary amendment.
    ☐ A SECOND or SUBSEQUENT preliminary amendment.

14. ☒ A substitute specification.

15. ☐ A change of power of attorney and/or address letter.

16. ☒ Other items or information:
    a. ☒ Submission of Drawings - 2 sheets
    b. ☒ Submission of Proposed Drawing Changes
    c. ☒ EXPRESS MAIL #EL843743170US dated November 15, 2001

IC13 Rec'd PCT/PTO 15 NOV 2001

U.S. APPLICATION NO. (if known, see 37 C.F.R. 1.5) 09/980317	INTERNATIONAL APPLICATION NO. PCT/DE00/01497	ATTORNEY'S DOCKET NUMBER P01,0345

17. ☒ The following fees are submitted:	CALCULATIONS	PTO USE ONLY
BASIC NATIONAL FEE (37 C.F.R. 1.492(a)(1)-(5):		
Search Report has been prepared by the EPO or JPO $890.00		
International preliminary examination fee paid to USPTO (37 C.F.R. 1.482) ... $670.00		
No international preliminary examination fee paid to USPTO (37 C.F.R. 1.482) but international search fee paid to USPTO (37 C.F.R. 1.445(a)(2) $760.00		
Neither international preliminary examination fee (37 C.F.R. 1.482) nor international search fee (37 C.F.R. 1.445(a)(2) paid to USPTO $970.00		
International preliminary examination fee paid to USPTO (37 C.F.R. 1.482) and all claims satisfied provisions of PCT Article 33(2)-(4) ..... $ 96.00		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$ 890.00	
Surcharge of $130.00 for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 C.F.R. 1.492(e)).	$	

Claims	Number Filed		Number Extra	Rate		
Total Claims	6	- 20 =	0	X $18.00	$	
Independent Claims	1	- 3 =	0	X $84.00	$	
Multiple Dependent Claims				$280.00 +	$	
TOTAL OF ABOVE CALCULATIONS =					$ 890.00	
Reduction by 1/2 for filing by small entity, if applicable. Verified Small Entity statement must also be filed. (Note 37 C.F.R. 1.9, 1.27, 1.28)					$	
SUBTOTAL =					$ 890.00	
Processing fee of $130.00 for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(f)). +					$	
TOTAL NATIONAL FEE =					$ 890.00	
Fee for recording the enclosed assignment (37 C.F.R. 1.21(h). The assignment must be accompanied by an appropriate cover sheet (37 C.F.R. 3.28, 3.31). $40.00 per property +					**SEE ATTACHED ENVELOPE**	
TOTAL FEES ENCLOSED =					$ 890.00	
					Amount to be refunded	$
					charged	$

☒ A check in the amount of $890.00 to cover the above fees is enclosed.

b ☐ Please charge my Deposit Account No. _____ in the amount of $ _____ to cover the above fees. A duplicate copy of this sheet is enclosed.

c ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. **501519**. A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 C.F.R. 1.494 or 1.495 has not been met, a petition to revive (37 C.F.R. 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

Schiff Hardin & Waite
Patent Department
600 Sears Tower
Chicago, Illinois 60606-6473
Customer Number 26574

James D. Hobart
SIGNATURE

James D. Hobart
NAME

24,149
Registration Number

CERTIFICATE OF MAILING BY U.S. EXPRESS MAIL

"Express Mail" Mailing Label Number EL843743170US

Date of Deposit: November 15, 2001

I hereby certify that this correspondence is being deposited with the United States Postal "Express Mail Post Office to Addressee" service under 37 CFR 1.10(c) on the date indicated above and is addressed to:

BOX PCT
Commissioner of Patents and Trademarks
Washington, D.C. 20231

Case Number: P01,0345

International Application No.
PCT/DE00/01497

International Filing Date
11 May 2000

Priority Date Claimed
20 May 1999

Title: "SUBSTRATE WITH AT LEAST TWO METALLIZED POLYMER BUMPS FOR SOLDERED CONNECTION TO WIRING"

Applicant(s): Jozef van Puymbroeck

Enclosed are the following documents:

International application as filed;
English translation of application;
Executed Declaration;
Information Disclosure Statement, PTO 1449,
Prior Art, Search Report;
Preliminary Amendment;
Substitute Specification;
Marked-up Copy of Specification;
Letter Submitting Drawings - 2 sheets;
Submission of Proposed Drawing Changes;
PTO 1390 in duplicate;
Filing Fee: $890.00;
Postcard.

Executed Assignment, PTO 1595 form, $40.00 filing fee, postcard, in attached envelope to be forwarded to the Assignment Branch.

M. Bellan

Signature of person mailing documents and fee

**IN THE UNITED STATES ELECTED OFFICE OF
THE UNITED STATES PATENT AND TRADEMARK OFFICE
UNDER THE PATENT COOPERATION TREATY - CHAPTER II**

PRELIMINARY AMENDMENT

APPLICANT: Jozef van Puymbroeck

ATTORNEY DOCKET NO.: P01,0345

SERIAL NO.: EXAMINER:

FILING DATE: ART UNIT:

INTERNATIONAL APPLICATION NO.: PCT/DE00/01497

INTERNATIONAL FILING DATE: 11 May 2000

INVENTION: "SUBSTRATE WITH AT LEAST TWO METALLIZED POLYMER BUMPS FOR SOLDERED CONNECTION TO WIRING"

BOX PCT
Assistant Commissioner for Patents
Washington, D.C. 20231

S I R:

Please amend the above-identified International Application before entry into the National Stage before the U.S. Patent and Trademark Office under 35 USC 371 as follows:

IN THE SPECIFICATION:

Please replace pages 1, 1a, 2, 2a, 3, 3a, 4, 4a, 5, 5a, 6, 6a, 7 and 8 with the attached Substitute Specification, which contains no new matter. The changes made to the specification are shown in the marked-up version, which is attached herewith as an appendix.

IN THE ABSTRACT:

Please replace the Abstract on page 9 of the translation with the attached unnumbered page containing an Abstract of the Disclosure. A marked-up version of the Abstract is attached herewith in the appendix.

IN THE CLAIMS:

Please amend claims 1-6 as follows:

--1. (Amended) A substrate having at least two metallized polymer studs for soldered connections to a wiring and having conductor runs which lead away from the polymer studs on a lower face of the substrate, each of the polymer studs having at least one step in order to form at least one projection.--

--2. (Amended) The substrate according to claim 1, wherein the projection is a cylindrical projection which is arranged concentrically with respect to the polymer stud.--

--3. (Amended) The substrate according to claim 2, wherein the cylindrical projection has a diameter of between 100μm and 300μm, and a height of between 25μm and 250μm.--

--4. (Amended) The substrate according to claim 1, wherein the polymer studs are provided with two projections forming two steps.--

--5. (Amended) The substrate according to claim 1, wherein the polymer studs are provided with a number of projections arranged at a distance from one another on the step.--

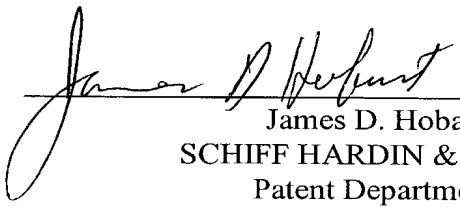
--6. (Amended) The substrate according to claim 1, wherein the polymer studs are provided with an annular projection arranged on the step.--

REMARKS

Claims 1-6 are presented for examination.

By this amendment, the translation of the original PCT Application has been amended to correct grammatical errors and to provide headings. These corrections are in the Substitute Specification, which contains no new matter, and the changes are shown in the marked-up version attached as an appendix. In addition, a new Abstract has been submitted and is attached herewith, with the changes in the Abstract being shown in the marked-up version attached as the appendix. Finally, claims 1-6 have been amended to remove the reference numerals and to place them in form for examination in the United States Patent Office. These amendments are shown in the appendix, with insertions being underlined and with portions being removed in brackets. It is submitted that the amendments to claims 1-6 do not change the indication of allowable subject matter set forth in the Preliminary Examination Report dated August 21, 2001.

Respectfully submitted,



(Reg. No. 24,149)

James D. Hobart
SCHIFF HARDIN & WAITE
Patent Department
6600 Sears Tower
233 South Wacker Drive
Chicago, Illinois 60606
Telephone: (312) 258-5781
Customer Number 26574

DATED: November 15, 2001

ABSTRACT OF THE DISCLOSURE

A substrate having at least two metallized polymer studs, in particular a polymer stud grid array, is designed so that the polymer studs have at least one step and at least one projection extending from the step. This geometry of the solder studs ensures reliable soldered connections to a wiring and reproducible layer thicknesses of the solder.

**IN THE UNITED STATES ELECTED OFFICE OF
THE UNITED STATES PATENT AND TRADEMARK OFFICE
UNDER THE PATENT COOPERATION TREATY - CHAPTER II**

SUBMISSION OF DRAWINGS

APPLICANT: Jozef van Puymbroeck

ATTORNEY DOCKET NO.: P01,0345

SERIAL NO.: EXAMINER:

FILING DATE: ART UNIT:

INTERNATIONAL APPLICATION NO.: PCT/DE00/01497

INTERNATIONAL FILING DATE: 11 May 2000

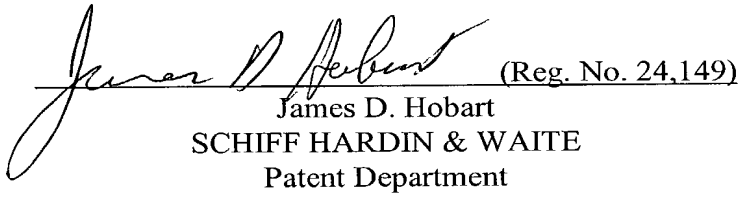
INVENTION: "SUBSTRATE WITH AT LEAST TWO METALLIZED POLYMER BUMPS FOR SOLDERED CONNECTION TO WIRING"

BOX PCT
Assistant Commissioner for Patents
Washington, D.C. 20231

S I R:

Attached herewith are two sheets of Formal Drawings containing Figs. 1-6.

Respectfully submitted,



(Reg. No. 24,149)

James D. Hobart
SCHIFF HARDIN & WAITE
Patent Department
6600 Sears Tower
233 South Wacker Drive
Chicago, Illinois 60606
Telephone: (312) 258-5781
Customer Number 26574

DATED: November 15, 2001

TITLE

"SUBSTRATE WITH AT LEAST TWO METALLIZED POLYMER STUDS FOR SOLDERING CONNECTIONS TO A WIRING"

BACKGROUND OF THE INVENTION

Integrated circuits are having ever greater numbers of connections, and are at the same time being even further miniaturized. The difficulties expected with this increase in miniaturisation with the application of solder paste and component placement are intended to be overcome by new package forms with either single-chip modules, few-chip modules or multi-chip modules preferably in a ball grid array package (see German periodical, Productronic, Vol. 5, 1994, pages 54, 55). These modules are based on a plated-through substrate, on which contact is made with the chips, for example, via contact-making wires or by means of flipchip mounting. On the lower face of the substrate, there is a ball grid array (BGA), which is frequently also referred to as a solder grid array or solder bump array. Ball grid arrays have solder studs arranged over the entire area of the lower face of the substrate, and these studs allow surface mounting on printed circuit boards or assemblies. The arrangement of the solder studs over the entire area allows a large number of connections to be provided in a coarse grid of, for example, 1.27 mm.

The use of what is referred to as MID technology, wherein MID means Molded Interconnection Devices, allows injection-molded parts with integrated conductor runs to be used rather than conventional printed circuits. High-quality thermoplastics which are suitable for injection molding of three-dimensional substrates are used as the basis for this technology. Thermoplastics such as these are characterized in comparison to conventional substrate materials for printed circuits

by having better mechanical, chemical, electrical and environmental characteristics. In one specific direction of MID technology, referred to as SIL technology, wherein SIL is German language abbreviation for "injection-molded parts with integrated conductor runs", a metal layer applied to the injection-molded parts is structured without any necessity for the otherwise normal mask technique by means of a special laser structuring process. In this case, a number of mechanical and electrical functions can be integrated in the three-dimensional injection-molded parts with a structured metallization. The package support functions are carried out at the same time by guides and snap-action connections, while the metallization layer is used for electromagnetic shielding in addition to the wiring and connection function, and the metallization layer ensures good heat dissipation. Appropriate plated-through holes are produced during the injection-molding process itself in order to provide electrically conductive cross-connections between two wiring systems on mutually opposite surfaces of the injection-molded parts. The inner walls of these plated-through holes are then likewise coated with a metal layer, during the metallization of the injection-molded parts. Further details relating to the production of the three-dimensional injection-molded parts with integrated conductor runs can be found, for example, in DE-A-37 32 249 or in EP-A-0 361 192.

A single-chip module is known from WO-A-89/00346, in which the injection-molded, three-dimensional substrate is composed of an electrically insulating polymer and, on its lower face, has studs which are formed at the same time during the injection-molding process and which studs can also be arranged over the entire surface, if required. An IC chip is arranged on the upper face of this substrate, and its connections are connected via fine bonding wires to interconnects formed on the upper face of the substrate. These interconnects are themselves

connected via plated-through holes to associated external connections formed on the studs.

What is referred to as a polymer stud grid array (PSGA) is known from WO-A-96/09646, and this combines the advantages of a ball grid array (BGA) with the advantages of MID technology. The use of the expression polymer stud grid array (PSGA) for the new type is based on the expression ball grid array (BGA), with the expression "polymer stud" being intended to indicate polymer studs that are formed at the same time as the injection molding of the substrate. The new type, which is suitable for either single-chip, few-chip or multi-chip modules, has

- an injection-molded, three-dimensional substrate composed of an electrically insulating polymer;
- polymer studs which are arranged over the entire area on the lower face of the substrate and are formed at the same time during the injection-molding process;
- external connections formed on the polymer studs by means of a detachable end surface;
- conductor runs which are formed at least on the lower face of the substrate and connect the external connections to the internal connections; and
- at least one chip which is arranged on the substrate and whose connections are electrically connected to the internal connections.

In addition to the simple and cost-effective production of the polymer studs during the injection-molding process for the substrate, the external connections on the polymer studs can also be produced with minimal effort, together with the normal production of the conductor runs as for MID technology or SIL technology. The fine

laser structuring, which is preferred for SIL technology, allows the large numbers of connections to be provided on the polymer studs, in a fine grid.

Another preferable factor is that the thermal expansion of the polymer studs corresponds to the thermal expansions of the substrate and of the wiring that holds the module. This results in highly reliable soldered connections even when temperature fluctuations occur frequently.

It is also known, from US-A-5 477 087, for the elastic characteristics and the temperature response of the polymer studs to be utilized for making contact with electronic components, such as semiconductors. To this end, a metal barrier layer is first of all in each case applied to the aluminum electrodes of the electronic components, and the polymer studs are then formed on these metal layers. The completely formed polymer studs are then coated with a layer of a metal which has a low melting point.

If polymer stud grid arrays or other components with metallized polymer studs are connected to wiring systems such as printed circuit boards, for example, by means of reflow soldering, then there is a risk of the molten solder being drawn upward along the metallization on the polymer studs. This phenomenon, which occurs with about 75% of the polymer studs, then, however, itself leads to nonreproducible solder layer thicknesses under the polymer studs and, possibly, to short circuits, to adjacent interconnects.

SUMMARY OF THE INVENTION

The invention is based on the problem of ensuring reproducible solder layer thicknesses under the polymer studs in the case of a substrate having polymer studs for soldered connections to a wiring system.

The invention is based on the knowledge that a polymer stud geometry having at least one projection forms a step or steps which makes it possible to prevent the molten solder from being drawn upward. This results in reproducible solder layer thicknesses under the polymer studs which, for their part, ensure highly reliable soldered connections. The risk of short circuits, which are caused by solder being drawn upward, can likewise be prevented.

The refinement of the stud is for the projection to be a concentric, cylindrical projection, which is suitable for production of substrates with integral polymer studs by means of injection molding. In this case, the dimensions of a cylindrical projection of a diameter between 100µm and 300µm and a height of between 25µm and 250 µm in a polymer stud grid array have led to particularly reliable soldered connections.

The variants for the geometry of the polymer studs, which include a projection with a second projection extending therefrom to form two steps, a number of projections, and an annular projection on the step, also prevent the solder from being drawn upward, by means of the steps. This results in the capability to match the geometry of the polymer studs to particular applications.

Exemplary embodiments of the invention are described in more detail in the following text and are illustrated in the drawing.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows a section, illustrated in cutaway form, through a substrate having integrally formed, stepped polymer studs,

Figure 2 shows a cross-section of a polymer stud on the substrate shown in Figure 1, with a metallization applied to it and with a conductor run leading away from the polymer stud,

Figure 3 shows a cross-section of a soldered connection of the polymer stud illustrated in Figure 2 to a wiring system,

Figure 4 shows a cross-section of a first variant of a polymer stud having a compound projection,

Figure 5 shows a cross-section of a second variant for the polymer studs, with a number of projections arranged on one step, and

Figure 6 shows a cross-section of a third variant for the polymer studs, with an annular projection.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figure 1 shows a section through a substrate S, on whose lower face U polymer studs PS, which are also formed during the injection molding of the substrate, are arranged in order to form a polymer stud grid array. As can be seen, the slightly conical polymer studs PS are each provided at their lower end with cylindrical projections E. The diameters of the cylindrical projections E are of such

a size that an annular step ST is in each case formed as the transition to the rest of the polymer stud PS. In the illustrated exemplary embodiment, a polymer stud PS has a diameter D of 400 μm in its base region, while the height H, as the distance between the lower face U of the substrate S and the step ST, is 400 μm. The diameter d of the cylindrical projection E is 160 μm, while the height h of the cylindrical projection E is 50 μm.

Figure 2 shows a polymer stud PS as shown in Figure 1 after a very-fine laser structuring of a metal layer which is applied to the entire surface of the substrate S. As can be seen, the polymer stud PS, including the cylindrical projection E, is provided with a metallization MB, and a conductor run LZ leads away from the polymer stud PS on the lower face U of the substrate S.

Figure 3 shows the soldered connection of the polymer stud PS, illustrated in Figure 2, to a wiring system V which, in the illustrated exemplary embodiment, is in the form of a printed circuit board LP with connecting pads AP arranged on the upper face. This clearly shows that all the solder L remains in the area between the step ST and the connecting pad AP during reflow soldering, and is not drawn up along the sides of the stud toward the conductor runs LZ, as in the case of polymer studs without a step. The geometry of the stepped polymer studs PS thus ensures reproducible layer thicknesses for the solder L.

In the first variant illustrated in Figure 4, a polymer stud PS1 is integrally formed on a substrate S1. A double step on the polymer studs PS1 results in an annular projection E1 and a cylindrical projection E10 being formed. This compound arrangement of two projections E1 and E10 forms annular steps ST1 and ST10.

In the second variant, which is illustrated in Figure 5, the polymer studs PS2 are integrally formed on a substrate S2. A total of four cylindrical projections E2, which are arranged spaced apart from one another, are provided on a step ST2 in the form of a platform.

In the third variant, which is illustrated in Figure 6, the polymer studs PS3 are integrally formed on a substrate S3. An annular projection E3 is in this case located on a step ST3, which is likewise in the form of a platform.

Apart from the slightly truncated conical polymer studs illustrated in Figures 1 to 6, polymer studs or projections with other cross-sectional shapes may also be used. However, the formation of at least one step which prevents the solder from being drawn up at the sides during reflow soldering is also of a critical importance.

I CLAIM:

**IN THE UNITED STATES ELECTED OFFICE OF
THE UNITED STATES PATENT AND TRADEMARK OFFICE
UNDER THE PATENT COOPERATION TREATY - CHAPTER II**

SUBMISSION OF PROPOSED DRAWING CHANGES

APPLICANT: Jozef van Puymbroeck

ATTORNEY DOCKET NO.: P01,0345

SERIAL NO.: EXAMINER:

FILING DATE: ART UNIT:

INTERNATIONAL APPLICATION NO.: PCT/DE00/01497

INTERNATIONAL FILING DATE: 11 May 2000

INVENTION: "SUBSTRATE WITH AT LEAST TWO METALLIZED POLYMER BUMPS FOR SOLDERED CONNECTION TO WIRING"

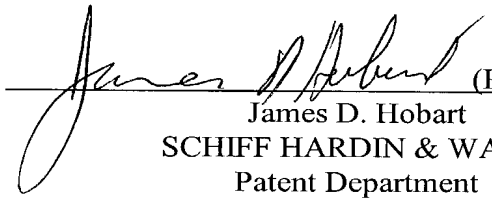
BOX PCT
Assistant Commissioner for Patents
Washington, D.C. 20231

S I R:

Applicant proposes to add cross-hatching to Figs. 1-6, which are cross-sectional views, and element numbers, as indicated in red.

If these corrections are approved, applicant will submit corrected Formal Drawings once the application has been allowed.

Respectfully submitted,



(Reg. No. 24,149)

James D. Hobart
SCHIFF HARDIN & WAITE
Patent Department
6600 Sears Tower
233 South Wacker Drive
Chicago, Illinois 60606
Telephone: (312) 258-5781
Customer Number 26574

DATED: November 15, 2001

FIG 1

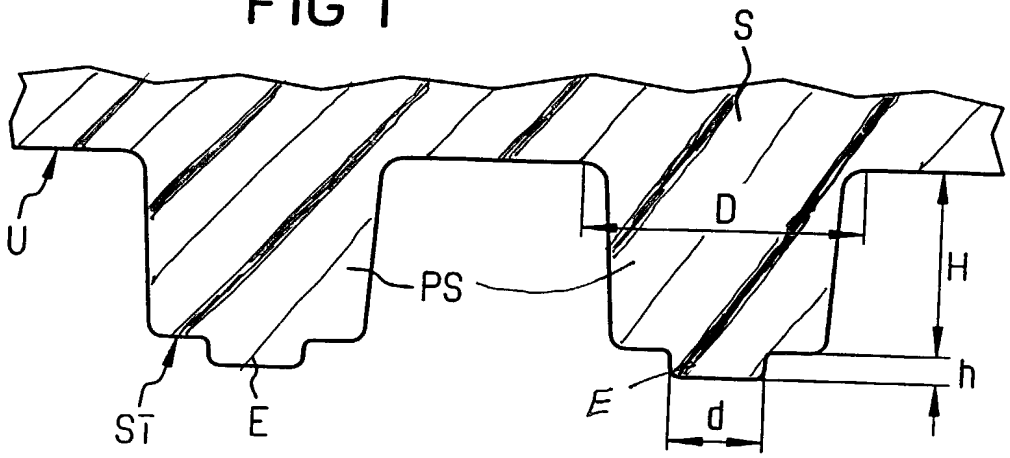


FIG 2

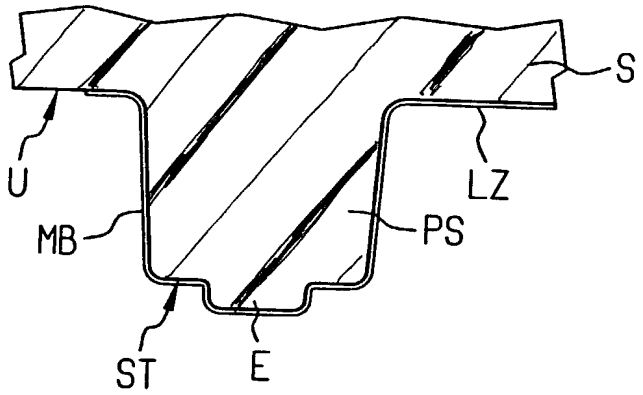


FIG 3

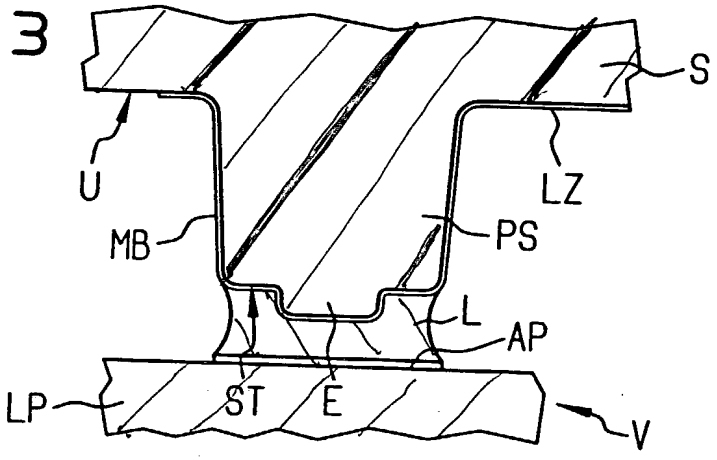


FIG 4

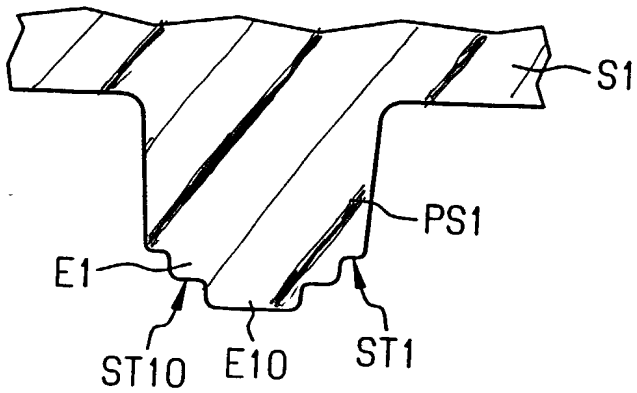


FIG 5

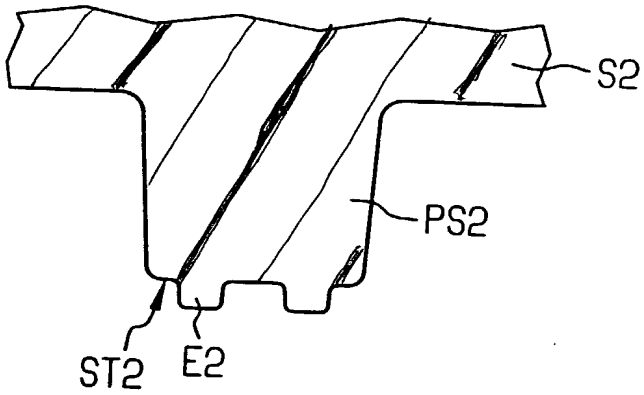
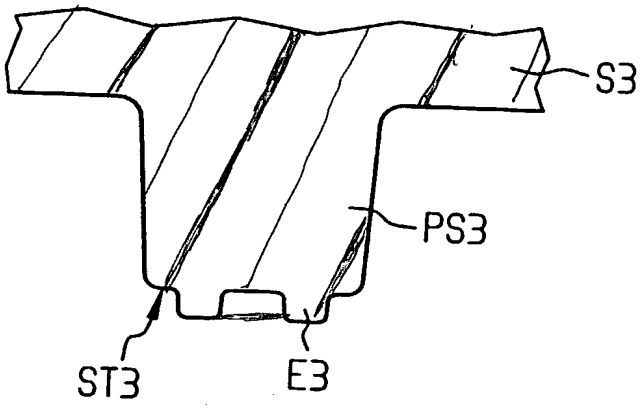


FIG 6



Description

Substrate having at least two metallized polymer studs for soldered connections to wiring

Integrated circuits are having ever greater numbers of connections, and are at the same time being ever further miniaturized. The difficulties expected with this increase in miniaturisation with the application of solder paste and component placement are intended to be overcome by new package forms, with single-chip modules, few-chip modules or multi-chip modules in a ball grid array package being preferred, in particular, in this case (DE-Z productronic 5, 1994, pages 54, 55). These modules are based on a plated-through substrate, on which contact is made with the chips, for example, via contact-making wires or by means of flipchip mounting. On the lower face of the substrate, there is a ball grid array (BGA), which is frequently also referred to as a solder grid array or solder bump array. Ball grid arrays have solder studs arranged over the entire area of the lower face of the substrate, and these allow surface mounting on printed circuit boards or assemblies. The arrangement of the solder studs over the entire area allows large numbers of connections to be provided in a coarse grid of, for example, 1.27 mm.

The use of what is referred to as MID technology (MID = Molded Interconnection Devices) allows injection-molded parts with integrated conductor runs to be used rather than conventional printed circuits. High-quality thermoplastics which are suitable for injection molding of three-dimensional substrates are used as the basis for this technology. Thermoplastics such as these are characterized in comparison to conventional substrate materials for printed circuits by having better mechanical, chemical, electrical and environmental characteristics. In one specific direction of MID

technology, referred to as SIL technology (SIL is a German abbreviation for injection-molded parts with integrated conductor runs), a metal layer applied to the injection-molded parts is structured without any necessity for the otherwise normal mask technique by means of a

special laser structuring process. In this case, a number of mechanical and electrical functions can be integrated in the three-dimensional injection-molded parts with structured metallization. The package support functions are carried out at the same time by guides and snap-action connections, while the metallization layer is used for electromagnetic shielding in addition to the wiring and connection function, and ensures good heat dissipation. Appropriate plated-through holes are produced during the injection-molding process itself in order to provide electrically conductive cross-connections between two wiring systems on mutually opposite surfaces of the injection-molded parts. The inner walls of these plated-through holes are then likewise coated with a metal layer, during the metallization of the injection-molded parts. Further details relating to the production of three-dimensional injection-molded parts with integrated conductor runs can be found, for example, in DE-A-37 32 249 or in EP-A-0 361 192.

A single-chip module is known from WO-A-89/00346, in which the injection-molded, three-dimensional substrate is composed of an electrically insulating polymer and, on its lower face, has studs which are formed at the same time during the injection-molding process and which can also be arranged over the entire surface, if required. An IC chip is arranged on the upper face of this substrate, and its connections are connected via fine bonding wires to interconnects formed on the upper face of the substrate. These interconnects are themselves connected via plated-through holes to associated external connections formed on the studs.

What is referred to as a polymer stud grid array (PSGA) is known from WO-A-96 096 46, and this combines the advantages of a ball grid array (BGA) with the advantages of MID technology. The use of the expression

polymer stud grid array (PSGA) for the new type is based on the expression ball grid array (BGA), with the expression "polymer stud" being intended to indicate polymer studs that are formed at the same time as the injection molding of the substrate. The

new type, which is suitable for single-chip, few-chip or multi-chip modules, has

- an injection-molded, three-dimensional substrate composed of an electrically insulating polymer,
- polymer studs which are arranged over the entire area and are formed at the same time during the injection-molding process, on the lower face of the substrate,
- external connections formed on the polymer studs by means of a detachable end surface,
- conductor runs which are formed at least on the lower face of the substrate and connect the external connections to the internal connections, and
- at least one chip which is arranged on the substrate and whose connections are electrically conductively connected to the internal connections.

In addition to the simple and cost-effective production of the polymer studs during the injection-molding process for the substrate, the external connections on the polymer studs can also be produced with minimal effort, together with the normal production of the conductor runs as for MID technology or SIL technology. The fine laser structuring which is preferred for SIL technology allows the large numbers of connections to be provided on the polymer studs, in a fine grid.

Another preferable factor is that the thermal expansion of the polymer studs corresponds to the thermal expansions of the substrate and of the wiring that holds the module. This results in highly reliable soldered connections even when temperature fluctuations occur frequently.

It is also known, from US-A-5 477 087, for the elastic characteristics and the temperature response of polymer

studs to be utilized for making contact with electronic components, such as semiconductors. To this end, a metal barrier layer is first of all in each case applied to the aluminum electrodes of the electronic components, with

polymer studs then being formed on these metal layers. The completely formed polymer studs are then coated with a layer of a metal which has a low melting point.

If polymer stud grid arrays or other components with metallized polymer studs are connected to wiring systems such as printed circuit boards, for example, by means of reflow soldering, then there is a risk of the molten solder being drawn upward along the metallization on the polymer studs. This phenomenon, which occurs with about 75% of polymer studs, then, however, itself leads to nonreproducible solder layer thicknesses under the polymer studs and, possibly, to short circuits, to adjacent interconnects.

The invention specified in claim 1 is based on the problem of ensuring reproducible solder layer thicknesses under the polymer studs in the case of a substrate having polymer studs for soldered connections to a wiring system.

The invention is based on the knowledge that a polymer stud geometry having at least one projection makes it possible to prevent the mold on the solder from being drawn upward, by means of the step or steps formed in this way. This results in reproducible solder layer thicknesses under the polymer studs which, for their part, ensure highly reliable soldered connections. The risk of short circuits caused by solder being drawn upward can likewise be prevented.

Advantageous refinements of the invention are specified in the dependent claims.

The refinement as claimed in claim 2, is particularly suitable for production of substrates with integral polymer studs by means of injection molding. In this

case, the dimensions specified in claim 3 for the cylindrical projections

in polymer stud grid arrays have led to particularly reliable soldered connections.

The variants for the geometry of the polymer studs specified in claims 4, 5 and 6 likewise prevent the solder from being drawn upward, by means of the steps. This results in the capability to match the geometry of the polymer studs to particular applications.

Exemplary embodiments of the invention are described in more detail in the following text and are illustrated in the drawing, in which:

Figure 1 shows a section, illustrated in cutaway form, through a substrate having integrally formed, stepped polymer studs,

Figure 2 shows a polymer stud on the substrate shown in Figure 1, with metallization applied to it and with a conductor run leading away from the polymer stud,

Figure 3 shows a soldered connection of the polymer stud illustrated in Figure 2 to a wiring system,

Figure 4 shows a first variant with a polymer stud having two studs,

Figure 5 shows a second variant for the polymer studs, with a number of projections arranged on one step, and

Figure 6 shows a third variant for the polymer studs, with an annular projection.

Figure 1 shows a section through a substrate S, on whose lower face U polymer studs PS, which are also

formed during the injection molding of the substrate, are arranged in order to form a

polymer stud grid array. As can be seen, the slightly conical polymer studs PS are each provided at their lower end with cylindrical projections E. The diameters of the cylindrical projections E are of such a size that an annular step ST is in each case formed as the transition to the rest of the polymer stud PS. In the illustrated exemplary embodiment, a polymer stud PS has a diameter D of 400 µm in its base region, while the height H, as the distance between the lower face U of the substrate S and the step ST, is 400 µm. The diameter d of the cylindrical projection E is 160 µm, while the height h of the cylindrical projection E is 50 µm.

Figure 2 shows a polymer stud PS as shown in Figure 1 after very-fine laser structuring of a metal layer which is applied to the entire surface of the substrate S. As can be seen, the polymer stud PS, including the cylindrical projection E, is provided with a metallization M, and a conductor run LZ leads away from the polymer stud PS on the lower face U of the substrate S.

Figure 3 shows the soldered connection of the polymer stud PS, illustrated in Figure 2, to a wiring system V which, in the illustrated exemplary embodiment, is in the form of a printed circuit board LP with connecting pads AP arranged on the upper face. This clearly shows that all the solder L remains in the area between the step ST and the connecting pad AP during reflow soldering, and is not drawn up as far as the conductor runs LZ at the sides, as in the case of polymer studs without a step. The geometry of the stepped polymer studs PS thus ensures reproducible layer thicknesses for the solder L.

In the first variant illustrated in Figure 4, the polymer studs which are integrally formed on a

substrate S1 are annotated PS. A double step on the polymer studs PS1 results in an annular projection E1 and a cylindrical

projection E10 being formed. The associated annular steps are annotated ST1 and ST10, respectively.

In the second variant, which is illustrated in Figure 5, the polymer studs which are integrally formed on a substrate S2 are annotated PS2. A total of four cylindrical projections E2, which are arranged spaced apart from one another, are provided on a step ST2 in the form of a platform.

In the third variant, which is illustrated in Figure 6, the polymer studs which are integrally formed on a substrate S3 are annotated PS3. An annular projection E3 is in this case located on a step ST3, which is likewise in the form of a platform.

Apart from the slightly truncated conical polymer studs illustrated in Figures 1 to 6, polymer studs or projections with other cross-sectional shapes may also be used. However, the formation of at least one step which prevents the solder from being drawn up at the sides during reflow soldering is also of critical importance here.

Patent Claims

1. A substrate (S; S1; S2; S3) having at least two metallized polymer studs (PS; PS1; PS2; PS3) for soldered connections to wiring (V) and having conductor runs (LZ) which lead away from the polymer studs (PS; PS1; PS2; PS3) on the lower face (U) of the substrate (S; S1; S2; S3), with the polymer studs (PS; PS1; PS2; PS3) having at least one step (ST; ST1, ST10; ST2; ST3) in order to form at least one projection (E; E1; E10; E2; E3).

2. The substrate (S) as claimed in claim, characterized by a cylindrical projection (E) which is arranged concentrically with respect to the polymer stud (PS).

3. The substrate (S) as claimed in claim 2, characterized in that the cylindrical projection (E) has a diameter (d) of between 100 µm and 300 µm, and a height (h) of between 25 µm and 250 µm.

4. The substrate (S1) as claimed in claim 1, characterized in that polymer studs (PS1) are provided, having two projections (E1; E10) and two steps (ST1; ST10).

5. The substrate (S2) as claimed in claim 1, characterized in that polymer studs (PS2) are provided, having a number of projections (E2) arranged at a distance from one another on a step (ST2).

6. The substrate (S3) as claimed in claim 1, characterized in that polymer studs (PS3) are provided, having annular projections (E3) arranged on a step (ST3).

Abstract

Substrate having at least two metallized polymer studs for soldered connections to wiring

A substrate (S) having at least two metallized polymer studs (PS), in particular a polymer stud grid array, is designed such that the polymer studs (PS) have at least one step (ST) and at least one projection (E). This geometry of the solder studs (PS) ensures reliable soldered connections to wiring (V) and reproducible layer thicknesses of the solder (L).

Figure 3

FIG 1

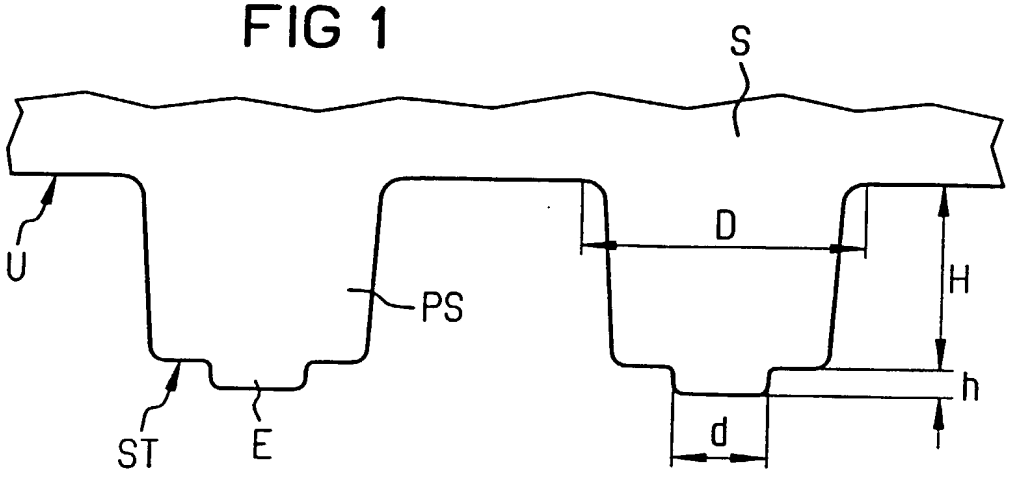


FIG 2

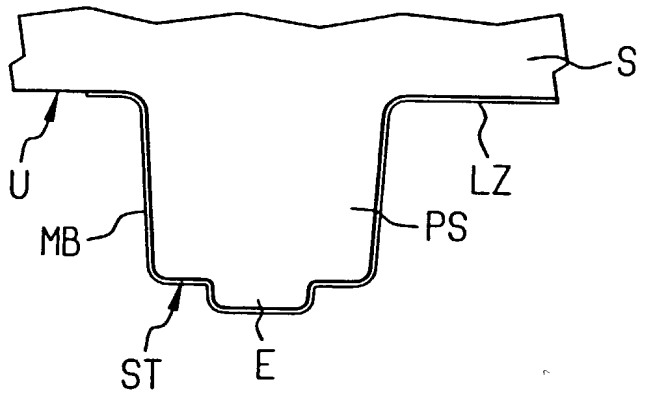


FIG 3

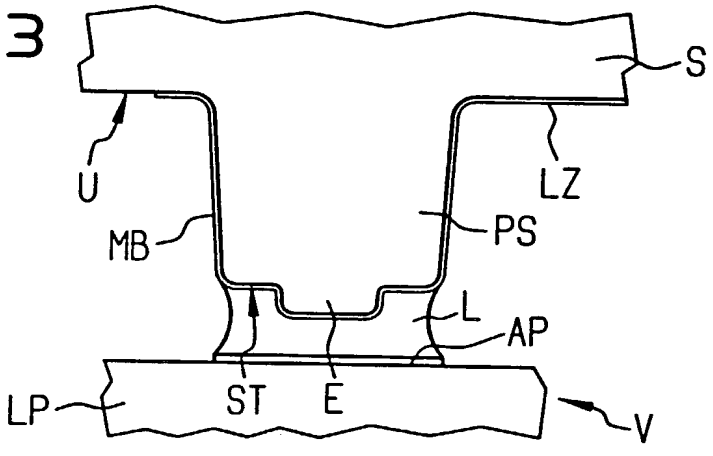


FIG 4

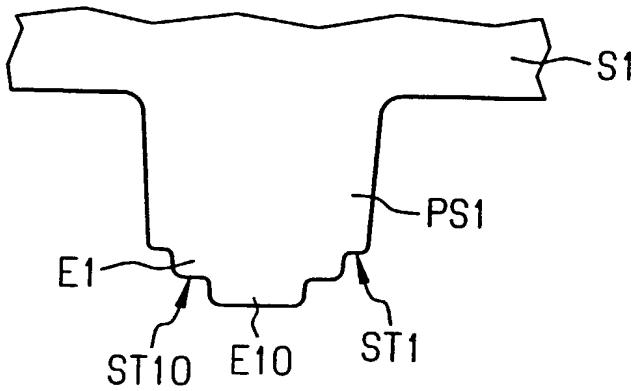


FIG 5

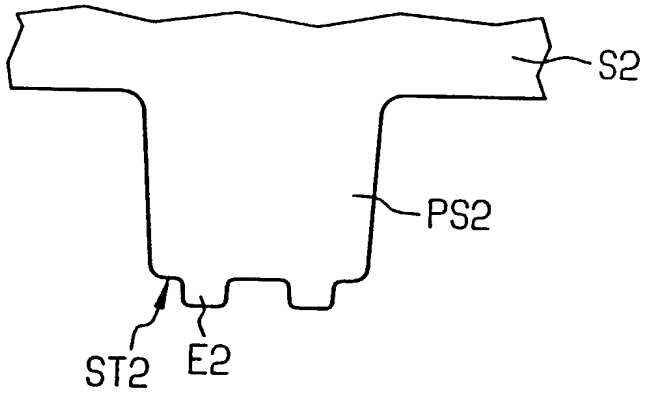
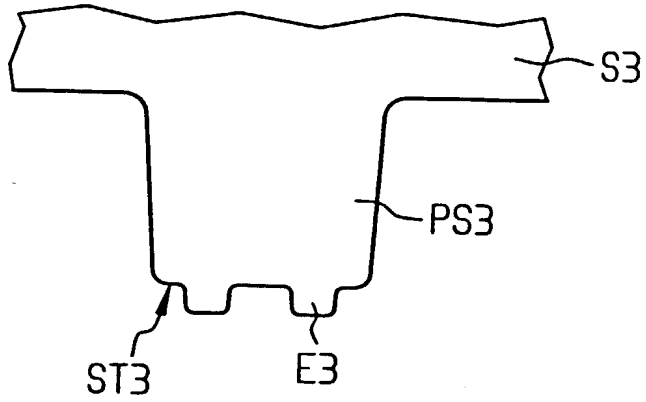


FIG 6



Declaration and Power of Attorney For Patent Application
Erklärung Für Patentanmeldungen Mit Vollmacht
German Language Declaration

Als nachstehend benannter Erfinder erkläre ich hiermit an Eides Statt:

As a below named inventor, I hereby declare that:

dass mein Wohnsitz, meine Postanschrift, und meine Staatsangehörigkeit den im Nachstehenden nach meinem Namen aufgeführten Angaben entsprechen,

My residence, post office address and citizenship are as stated below next to my name,

dass ich, nach bestem Wissen der ursprüngliche, erste und alleinige Erfinder (falls nachstehend nur ein Name angegeben ist) oder ein ursprünglicher, erster und Miterfinder (falls nachstehend mehrere Namen aufgeführt sind) des Gegenstandes bin, für den dieser Antrag gestellt wird und für den ein Patent beantragt wird fur die Erfindung mit dem Titel:

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

Substrat mit mindestens zwei metallisierten Polymerhoeckern fuer die Loetverbindung mit einer Verdrahtung

Substrate with at least two metallized polymer bumps for soldered connection to wiring

deren Beschreibung

the specification of which

(zutreffendes ankreuzen)
☐ hier beigefügt ist.
☒ am 11 05 2000 als
PCT internationale Anmeldung
PCT Anmeldungsnummer PCT/DE00/01497
eingereicht wurde und am _____
abgeändert wurde (falls tatsächlich abgeändert).

(check one)
☐ is attached hereto.
☒ was filed on 11.05.2000 as
PCT international application
PCT Application No. PCT/DE00/01497
and was amended on _____
(if applicable)

Ich bestatige hiermit, dass ich den Inhalt der obigen Patentanmeldung einschliesslich der Ansprüche durchgesehen und verstanden habe, die eventuell durch einen Zusatzantrag wie oben erwähnt abgeändert wurde.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims as amended by any amendment referred to above.

Ich erkenne meine Pflicht zur Offenbarung irgendwelcher Informationen, die für die Prüfung der vorliegenden Anmeldung in Einklang mit Absatz 37, Bundesgesetzbuch, Paragraph 1.56(a) von Wichtigkeit sind, an.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

Ich beanspruche hiermit ausländische Prioritätsvorteile gemäss Abschnitt 35 der Zivilprozessordnung der Vereinigten Staaten, Paragraph 119 aller unten angegebenen Auslandsanmeldungen für ein Patent oder eine Erfindersurkunde, und habe auch alle Auslandsanmeldungen für ein Patent oder eine Erfindersurkunde nachstehend gekennzeichnet, die ein Anmeldedatum haben, das vor dem Anmeldedatum der Anmeldung liegt, für die Priorität beansprucht wird.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

German Language Declaration

Prior foreign applications Priorität beansprucht			Priority Claimed	
19923247.4 (Number) (Nummer)	DE (Country) (Land)	20.05.1999 (Day Month Year Filed) (Tag Monat Jahr eingereicht)	☒ Yes Ja	☐ No Nein
(Number) (Nummer)	(Country) (Land)	(Day Month Year Filed) (Tag Monat Jahr eingereicht)	☐ Yes Ja	☐ No Nein
(Number) (Nummer)	(Country) (Land)	(Day Month Year Filed) (Tag Monat Jahr eingereicht)	☐ Yes Ja	☐ No Nein

Ich beanspruche hiermit gemäss Absatz 35 der Zivilprozessordnung der Vereinigten Staaten, Paragraph 120, den Vorzug aller unten aufgeführten Anmeldungen und falls der Gegenstand aus jedem Anspruch dieser Anmeldung nicht in einer früheren amerikanischen Patentanmeldung laut dem ersten Paragraphen des Absatzes 35 der Zivilprozeßordnung der Vereinigten Staaten, Paragraph 122 offenbart ist, erkenne ich gemäss Absatz 37, Bundesgesetzbuch, Paragraph 1.56(a) meine Pflicht zur Offenbarung von Informationen an, die zwischen dem Anmeldedatum der früheren Anmeldung und dem nationalen oder PCT internationalen Anmeldedatum dieser Anmeldung bekannt geworden sind.

I hereby claim the benefit under Title 35. United States Code. §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §122, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occured between the filing date of the prior application and the national or PCT international filing date of this application.

PCT/DE00/01497 (Application Serial No.) (Anmeldeseriennummer)	11.05.2000 (Filing Date D, M, Y) (Anmeldedatum T, M, J)	anhangig (Status) (patentiert, anhangig, aufgegeben)	pending (Status) (patented, pending, abandoned)
_____ (Application Serial No.) (Anmeldeseriennummer)	(Filing Date D,M,Y) (Anmeldedatum T, M; J)	_____ (Status) (patentiert, anhängig, aufgeben)	(Status) (patented, pending, abandoned)

Ich erkläre hiermit, dass alle von mir in der vorliegenden Erklärung gemachten Angaben nach meinem besten Wissen und Gewissen der vollen Wahrheit entsprechen, und dass ich diese eidesstattliche Erklärung in Kenntnis dessen abgebe, dass wissentlich und vorsätzlich falsche Angaben gemäss Paragraph 1001, Absatz 18 der Zivilprozessordnung der Vereinigten Staaten von Amerika mit Geldstrafe belegt und/oder Gefängnis bestraft werden koennen, und dass derartig wissentlich und vorsätzlich falsche Angaben die Gültigkeit der vorliegenden Patentanmeldung oder eines darauf erteilten Patentes gefährden können.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

German Language Declaration

VERTRETUNGSVOLLMACHT: Als benannter Erfinder beauftrage ich hiermit den nachstehend benannten Patentanwalt (oder die nachstehend benannten Patentanwälte) und/oder Patent-Agenten mit der Verfolgung der vorliegenden Patentanmeldung sowie mit der Abwicklung aller damit verbundenen Geschäfte vor dem Patent- und Warenzeichenamt: *(Name und Registrationsnummer anführen)*

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(list name and registration number)*

And I hereby appoint

Customer No. 26574

Telefongespräche bitte richten an: *(Name und Telefonnummer)*

Direct Telephone Calls to: *(name and telephone number)*

Ext. _____

Postanschrift:

Send Correspondence to.

Schiff, Hardin & Waite
6600 Sears Tower 60606-6473 Chicago, Illinois
Telephone: (001) 312 258 5780 and Facsimile (001) 312 258 5921
or
Customer No. 26574

Voller Name des einzigen oder ursprünglichen Erfinders:	Full name of sole or first inventor:
JOZEF VAN PUYMBROECK	JOZEF VAN PUYMBROECK
Unterschrift des Erfinders Datum: J. Van Puymbroeck 04.10.01	Inventor's signature Date
Wohnsitz: B-8020 OOSTKAMP, BELGIEN	Residence: B-8020 OOSTKAMP, BELGIUM BEX
Staatsangehörigkeit: BE	Citizenship: BE
Postanschrift: KORENBLOEMSTRAAT 17 B-8020 OOSTKAMP	Post Office Addess: KORENBLOEMSTRAAT 17 B-8020 OOSTKAMP
Voller Name des zweiten Miterfinders (falls zutreffend):	Full name of second joint inventor, if any:
Unterschrift des Erfinders Datum	Second Inventor's signature Date
Wohnsitz ,	Residence ,
Staatsangehörigkeit	Citizenship
Postanschrift	Post Office Address

(Bitte entsprechende Informationen und Unterschriften im Falle von dritten und weiteren Miterfindern angeben).

(Supply similar information and signature for third and subsequent joint inventors).